AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A data transmission system, comprising:

a primary board;

secondary boards; and

a data transmission path carrying out data transmission/reception between the primary board and the secondary boards, the data transmission path employs a same signal line as an address bus and a data bus mutually,

wherein when the data access is executed from the primary board to the secondary boards, informing a start address required for data access, and wherein an address used in the data access in the secondary boards is generated based on the start address, a predetermined trigger signal and a cycle signal indicating switching of data, the cycle signal is combined with the trigger signal, and

wherein the cycle signal counts plural times a leading edge of a clock signal of the primary board prior to toggle of the cycle signal.

2. (canceled).

3. (original): The data transmission system according to claim 1, wherein, when the address is generated based on the trigger signal, the address is generated sequentially by incrementing the start address in response to a timing of the trigger signal.

4. (canceled).

5. (currently amended): A data transmission system comprising:

a primary board;

secondary boards; and

a data transmission path for carrying out data transmission/reception between the primary board and the secondary boards, where the data transmission path employs a same signal line as an address bus and a data bus mutually,

wherein:

when the data access is executed from the primary board to the secondary boards, informing a memory start address of the secondary boards required for data access,

judging in the secondary boards whether or not the memory start address is directed to own station, and then executing the data transmission via the data transmission path by accessing a memory in own station based on the memory start address when the memory start address is directed to own station, and

an address is generated, to which the data transmission is subsequently executed, in the secondary boards by incrementing the memory start address after the data transmission

based on the memory start address is ended, and then executing the data transmission via the data transmission path by accessing the memory of own station based on the generated address,

wherein a cycle signal indicating switching of data is used in combination with a trigger signal,

wherein, when ~~a waveform is deformed by~~ disturbances are generated on the trigger signal during the data transmission/reception, the memory start address is not incremented, and

wherein the secondary board does not shift to a next process until the cycle signal has been toggled, and leading and trailing edges of the trigger signal are detected in combination with detecting the toggle states of the cycle signal,

wherein the cycle signal counts plural times a leading edge of a clock signal of the primary board prior to toggle of the cycle signal.

6. (currently amended): A method of transmitting data by a data transmission system comprising a primary board, secondary boards, and a data transmission path for carrying out data read between the primary board and the secondary boards, wherein the data transmission path employs a same signal line as an address bus and a data bus mutually, the method comprising::

informing a trigger signal combined with a cycle signal indicating a timing of data access, and a start address required for data read via the data transmission path;

switching the data transmission path to which the start address is informed as a data bus;

accessing a memory based on the start address and sending out a read result onto the data transmission path; and

incrementing the start address at a timing of the trigger signal, and then sending out a read result onto the data transmission path by accessing the memory based on the incremented address,

wherein the start address is not incremented when a waveform is deformed by the trigger signal during the data read, and

wherein the secondary board does not shift to a next process until the cycle signal has been toggled, and leading and trailing edges of the trigger signal are detected in combination with detecting the toggle states of the cycle signal,

wherein the cycle signal counts plural times a leading edge of a clock signal of the primary board prior to toggle of the cycle signal.

7. (canceled).

8. (currently amended): A data transmission system comprising:

a primary board;

secondary boards; and

a data transmission path for carrying out data write between the primary board and the secondary boards, where the data transmission path employs a same signal line as an address bus and a data bus mutually,

wherein the carrying out of the data write is executed by:

informing a trigger signal combined with a cycle signal indicating a timing of data access and a start address required for data write via the data transmission path,

switching the data transmission path to which the start address is informed as a data bus, and then sending out a predetermined data to be written to a memory;

accessing the memory based on the start address, and then writing the predetermined data into the memory,

incrementing the start address at a timing of the trigger signal, and then writing sequentially the predetermined data, that are sent out via the data transmission path, into the memory by accessing the memory based on the incremented address,

detecting leading and trailing edges of the trigger signal in combination with detecting toggle states of the cycle signal,

not incrementing the start address when a waveform is deformed by the trigger signal during the data write, and

not shifting the secondary board to a next process until the cycle signal has been toggled,

wherein the cycle signal counts plural times a leading edge of a clock signal of the primary board prior to toggle of the cycle signal.

9. (canceled).

10. (currently amended): A method for carrying out data write between a primary board and secondary boards by using a data transmission path, which employs a same signal line as an address bus and a data bus mutually, comprising:

informing a trigger signal combined with a cycle signal indicating a timing of data access and a start address required for data write via the data transmission path;

switching the data transmission path to which the start address is informed as a data bus, and then sending out a predetermined data to be written to a memory;

accessing the memory based on the start address, and then writing the predetermined data into the memory; and

incrementing the start address at a timing of the trigger signal, and then writing sequentially the predetermined data, that are sent out via the data transmission path, into the memory by accessing the memory based on the incremented address,

wherein the cycle signal counts plural times a leading edge of a clock signal of the primary board prior to toggle of the cycle signal.

11. (previously presented): The transmission system according to claim 1, wherein the cycle signal only indicates the switching of the data.

12. (currently amended): The transmission system according to claim 1, wherein the ~~trigger~~ cycle signal is a separate toggle signal having only two states and wherein the trigger

signal illustrates write and read timing of the data transmission pathis ~~toggled only in response to switching state of the cycle signal~~.

13. (previously presented): The transmission system according to claim 1, wherein the secondary board generates subsequent addresses used in data access based on the start address and wherein the subsequent addresses are generated by the secondary board by incrementing last address used.

14. (new): The transmission system according to claim 12, wherein the cycle signal is not a portion of an address and wherein the address is transmitted only in the address bus.